LOW K DIELECTRIC SURFACE DAMAGE CONTROL

FIELD OF THE INVENTION

[0001] The present invention relates to a method of forming a copper damascene structure in a semiconductor device and more particularly to a method of removing a silicon nitride or a nitride-based bottom etch stop layer in a copper damascene structure having a porous low K interlayer dielectric.

BACKGROUND OF THE INVENTION

[0002] In the conventional process for forming copper damascene structures in semiconductor devices, after the damascene opening has been etched into the porous low-k interlayer dielectric (ILD), the bottom etch stop layer is etched with a dry etch process before the damascene opening is filled with copper metal. A number of materials may be used for the bottom etch stop layer. Silicon carbide and silicon nitride are examples of materials commonly used for this purpose. Where the bottom etch stop layer is silicon nitride, the dry etch process conventionally practiced is plasma etch with a bias power. However, this etch process is generally conducted with a very low bias power because any overetch of the silicon nitride layer will cause undesirable back sputtering of the underlying copper in to the via. Such back sputtering of the underlying copper is not desirable because the sputtered extraneous copper deposits on the sidewalls of the low-k ILD can cause reliability problems.

[0003] Thus, improved method of etching the silicon nitride bottom etch stop layer in a copper damascene structure is desired. The concerns discussed herein are equally applicable to single damascene structures, copper via step structures, and copper dual damascene structures (with or without an intermediate etch stop layer).

SUMMARY OF THE INVENTION

[0004] According to an embodiment of the present invention, disclosed herein is a method of removing a nitride-based bottom etch stop layer in a copper damascene structure by etching the bottom etch stop layer using a high density, high radical

concentration plasma containing fluorine and oxygen. The copper damascene structure may be a via step, a single damascene structure, a dual damascene structure, or a non-intermediate etch stop layer dual damascene structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1 is a sectional illustration of a non-intermediate etch stop layer dual damascene structure at an interim process step before the removal of the bottom etch stop layer; and

[0006] Figure 2 is a sectional illustration of the non-intermediate etch stop layer dual damascene structure of Figure 1, after the bottom etch stop layer has been removed.

DETAILED DESCRIPTION

[0007] According to an embodiment of the present invention, disclosed herein is an etch process for removing a nitride-based bottom etch stop layer in a copper damascene structure. The method according to the present invention is applicable to a variety of copper damascene structures, such as, for example, a single damascene, a dual damascene, a non-intermediate etch stop layer dual damascene, and a via step structures.

[0008] Figure 1 illustrates a typical non-intermediate etch stop layer dual damascene structure at an interim stage of processing where a trench **10** and a via **20** openings have been formed in low-k interlayer dielectric (ILD) **30** but bottom etch stop layer **40** is still intact. Various other materials may be used for bottom etch stop layers but the method of the present invention is applicable to those copper damascene structures utilizing a nitride-based bottom etch stop layer. The bottom etch stop layer **40** may be formed of silicon nitride or other nitride-based materials such as oxynitride, a mixture of silicon oxide and silicon.

[0009] According to an embodiment of the present invention the bottom etch stop layer **40** at the bottom of the via **20** is etched using a high density, high radical concentration plasma containing fluorine and oxygen. The high radical concentration in the plasma is defined as having a radical-to-ion ratio equal to or greater than about 10:1.

[0010] By keeping the amount of ion in the plasma low, back sputtering of the copper underneath the bottom etch stop layer is minimized and also minimize the

physical damage to the surface of the low-k ILD by the plasma. If the radical-to-ion ratio is less than about 10:1 there is a greater likelihood that the underlying copper **50** will back sputter and deposit on the low-k ILD sidewalls of the damascene via **20**, which may cause reliability issues. Also, plasma containing higher ion content has a tendency to cause physical damage on the exposed horizontal surface **35** of the low-k ILD in the dual damascene structure during the etch process producing a rough low-k ILD surface. The rough surface is not desirable because it will increase the copper layer's sheet resistance, Rs, in the final copper damascene structure, especially in narrow lines.

[0011] In a preferred embodiment of the present invention, high density plasma may be produced utilizing one of a variety of available methods, such as, for example, inductive coupling plasma, electron cyclotron resonance, helicon wave, surface wave, and some capacitive coupling plasma, and microwave plasma tool. Use of high density plasma source is to have high dissociation to create more free fluorine or oxygen radical. High radical concentration is helpful for controlling the bottom etch stop layer's edge profile around the etched area. When the bottom etch stop layer **40** is removed from the bottom of the via **20** using the high radical-to-ion ratio plasma containing fluorine and oxygen, the edge profile of the bottom etch stop layer around the opening is vertical rather than tapered. The fluorine in the plasma may be provided by at least one of CF_4, CHF_3, SF_6, NF_3, C_2F_6, C_4F_8, CH_2F_2, CH_3F, and C_4F_6. High radical concentration also increases the etching process throughput.

[0012] By using a high density, high radical-to-ion ratio plasma containing fluorine and oxygen, a more chemical and less physical plasma etching is achieved, thus effectively removing the nitride-based bottom etch stop layer while minimizing the back sputter of the underlying copper and the surface damage of the low-k ILD in the damascene opening formed by the trench **10** and via **20**. Figure 2 illustrates the non-intermediate etch stop layer dual damascene structure of Figure 1 just after the bottom etch stop layer **40** has been etched away using the process according to an embodiment of the present invention from the bottom of the via **20**.

[0013] While the foregoing invention has been described with reference to the above embodiments, various modifications and changes can be made without departing

from the spirit of the invention. Accordingly, all such modifications and changes are considered to be within the scope of the appended claims.